A MIXER COMPUTER-AIDED DESIGN TOOL BASED IN THE TIME DOMAIN

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ABSTRACT

A time domain based technique for computer-aided mixer analysis and design is presented. The design tool uses SPICE (13) to arrive at the steady state solution for the network equations in the mixer circuit. These non-sinusoidal waveforms are studied to understand the interaction of diode, circuit and drive conditions. Graphically derived criteria are developed to optimize mixer performance. Circuit characteristics such as conversion loss, input and output impedances at any small-signal frequencies are rapidly calculated by using a Fast Hartley Transform (FHT) to generate the Fourier transform of the required waveforms (2). This technique can be used to analyze mixers that can be described in terms of transmission lines, lumped components or any other element blocks available with SPICE. As MMIC's are frequently designed with lumped components (10), it is envisaged that this tool could be applied to their design.

INTRODUCTION

In this paper we describe our approach to mixer design, compare it to the conventional mixer analysis technique - based predominately on a frequency domain description of the circuit and diode - and use this tool to design several broadband mixers. (Here a broadband circuit refers to a circuit that provides the same match at the RF frequency and the image frequency.) We consider diode mixers where the diodes are purely resistive or where they possess both barrier resistance and capacitance. Examples of single-ended and balanced mixers are given. The design of a phasing circuit which parametrically pumps the barrier capacitor in such a way as to improve conversion loss upon that of the purely resistive diode mixer is described. Lastly we compare our conversion loss results against those predicted using frequency domain analysis (5).

The flowchart of the program is shown in Fig. 1. Two types of programs operate on the SPICE generated time waveforms. One generates plots of diode and circuit variables, computes diode parameters and differential currents, and plots the energy waveforms in the circuit. The other quantitatively analyzes the mixer circuit by rapidly taking FHT's of the appropriate waveforms.

RESISTIVE MIXER DESIGN

Fig. 2 points out the similarities between a diode mixer and a idealized switching mixer. The local oscillator can be thought of as closing and opening a switch that allows the RF current source to reach a load resistor. The current in the load, I_L, and its value averaged over one LO period, $< I_L(t) >$, are plotted in the figure. $< I_L(t) >$ is maximized when the RF and LO are in phase, at T_1; its value can be used to calculate the output voltage at the difference frequency and thereby estimate the mixer's conversion loss, C_L.

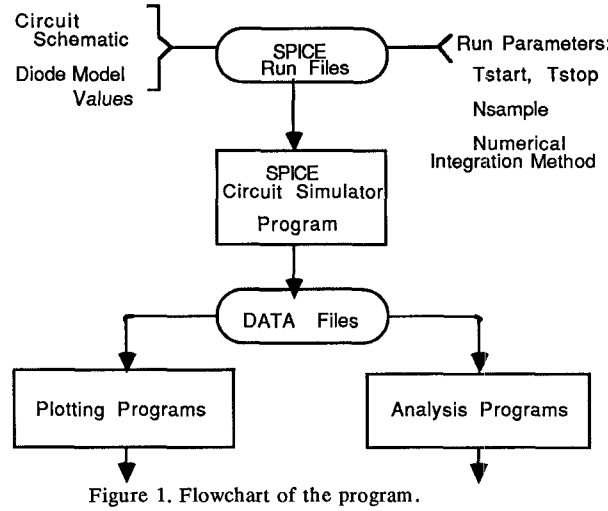

Figure 1. Flowchart of the program.

$$Vout(f_{IF}) = < I_L(T_1) > *R_L \quad (1)$$

$$C_L = \frac{I_{RF}{}^2 * R_S * R_L}{4 * Vout(f_{IF})^2} \quad (2)$$

This simple system is studied to examine C_L vs. switch duty cycle (comparable to the ratio of diode 'ON' time to LO period) or vs. choice of R_S and R_L.

$$Vout(f_{IF}) = \frac{1}{T_{LO}} * \int_0^{T_{LO}/2} I_{RF} \sin(w_{RF} t)\, dt * \frac{R_S R_L}{R_S + R_L} \quad (3)$$

$$Vout(f_{IF}) = I_{RF} * \frac{1}{\pi} * \frac{R_S R_L}{R_S + R_L} \qquad \text{for} T_{LO} = T_{RF} \quad (4)$$

For $f_{RF} \cong f_{LO}$, the optimum C_L can be mathematically shown to be 9.9dB when the switch duty cycle is 50% and $R_S = R_L$, independent of the value of R_S. Substitution of a purely resistive diode in place of the switch results in a C_L of 10.25dB; C_L is minimized when T_{ON}/T_{LO} is .50 and R_S is equal to R_L, as with the switch. Most importantly, the analogy between the switching mixer and a diode mixer allows one to see the importance of maximizing $< I_L(T_1) >$ to obtain low C_L. This performance criterion holds whether the diode has barrier capacitance or not.

We now look at the design of a simple broadband single-ended mixer when a purely resistive diode is used. If all out-of-band frequencies were reactively terminated, such a circuit would possess a C_L limit of 3dB (12); if not, the C_L limit is 3.9dB (6). The latter circuit is called a resistively matched circuit; its diagram and corresponding SPICE run file are shown in Fig. 3. Our application is the design of a mobile receiver using a direct downconversion scheme: the RF frequency is 909MHz, the IF is a few KHz, and the load impedance into which the mixer operates can be considered to be between 1K to 5KΩ. Because the diode is purely

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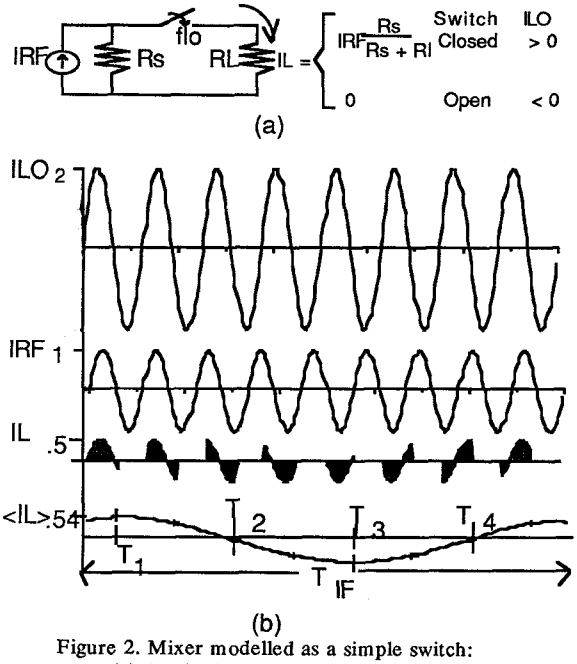

Figure 2. Mixer modelled as a simple switch: (a) circuit diagram; (b) waveforms.

resistive, the performance of the single-ended and balanced mixers discussed holds when higher frequencies are used. To maintain the number of time points per T_{IF} to a manageable size, we consider f_{IF} to be 1/100 of f_{RF}. R_S and R_L are set equal to minimize C_L; they are arbitrarily set to 1KΩ. It is possible to choose other source and load impedances and maintain similar C_L performance providing the drive, or LO, level is adjusted.

The output voltage for the resistively matched mixer and its spectrum are given in Fig. 4. C_L is calculated to be 4.3dB. It can be calculated from $< I_L(T_1)>$ (due to I_{RF}) from eqns.' (1) and (2) or found from the FHT of vout(t). Both methods agree to within 3%. The flow of RF current into the diode, R_S, and L_S can be examined to study the performance of the mixer. This is accomplished by subtracting the 180 deg. out-of-phase currents from the in-phase currents in the diode, R_S, and, L_S to obtain only the RF components when the LO and RF are in phase. These in-phase differential currents are shown in Fig. 5. The decomposition of I_{RF} into I_{diode}, I_{Rs}, and, I_{Ls} is also plotted when the RF and LO sources

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SINGLE ENDED MIXER
IBIAS 0 21 DC 0.0
VIMB 21 15
ILO 0 7 SIN(0 4.0M 900MEG)
VIM0 7 15
IRF 0 8 SIN(0 .4M 909MEG)
VIMR 8 15
VIMT 15 13
VIM1 13 12
RP 12 0 1000
LP 12 0 1.8UH
VIM2 13 9
VIM3 9 6
D1 6 3 DIODE1
RPD 9 3 5MEG
VIM4 3 23
RL 23 0 1000
VIM6 23 20
C1 20 0 2.8PF
.MODEL DIODE1 D RS=10.0 IS=1.0E-14 N=1.0 CJO=.001PF VJ=.9 BV=20
.OPTIONS ACCT OPTS NOPAGE ITL3=10 ITL5=160000 LVLTIM=1 LIMPTS=40000
.TRAN 27.13P .222US .111US
.PRINT TRAN V(3) I(VIM3) V(6,3) I(VIM2) V(13) V(0) V(0) V(0)
* Maximum parameters printed in one row is 8.
.END
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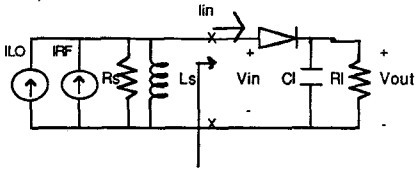

Figure 3. Resistively matched single-ended mixer: circuit diagram and corresponding SPICE run file.

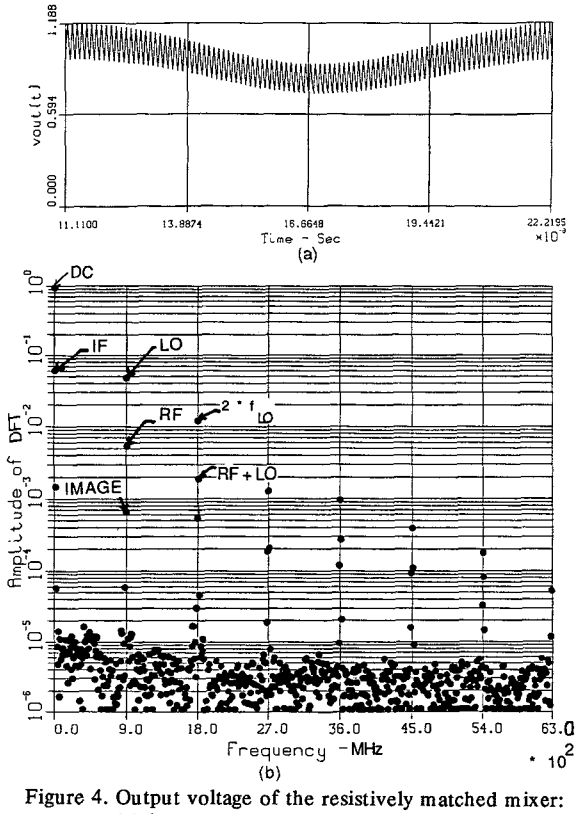

Figure 4. Output voltage of the resistively matched mixer: (a) time domain; (b) frequency domain.

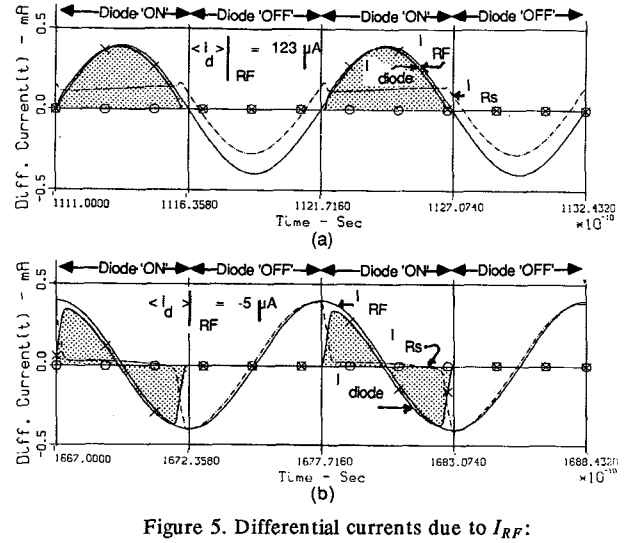

Figure 5. Differential currents due to I_{RF}: (a) in-phase; (b) quadrature-phase.

are in quadrature. This graphical data, remarkably similar to that of Fig. 2, highlights certain characteristics of the design that are key to attaining low conversion loss. First, the diode 'ON' time is set by the bias and drive sources to maximize $< I_L(T_1)>$, here T_{ON} is .5 T_{LO}. Second, when the diode is turned 'ON' $I_{RF} \cong I_{diode}$.

Fig. 6 gives the balanced version of the circuit shown in Fig. 3. The transformer is modelled as ideal, with coupling coefficient equal to 1.0 and inductor values as large as possible to reduce current flow. Bias can be achieved in practice by rectifying the LO

current and has been directly modelled with SPICE. To allow independent setting of I_{LO} and V_{bias}, bias is modelled as a series voltage supply. The output voltage and its spectrum are plotted in Fig. 7 when matched diodes are used. Conversion loss is identical to that obtained with the single-ended design and no DC or LO harmonics appear at the output. The level of LO harmonics at the output has been studied as a function of diode mismatch.

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SINGLE BALANCED MIXER
ILO 0 18 SIN(0 4M 900MEG)
VIM0 18 20
R1 20 0 1000
VIM1 20 15
RSER1 15 10 10.0
L1 10 0 10.0H
L2 30 40 10.0H
L3 40 45 10.0H
K1 L1 L2 1.0
K2 L1 L3 1.0
K3 L2 L3 1.0
RSER2 30 31 10.0
VBAT1 32 31 -0.5
VIM2 32 35
VIM5 35 37
D1 37 70 DIODE1
RPD1 35 70 5MEG
VBAT2 45 46 -0.5
RSER3 46 47 10.0
VIM3 47 49
VIM6 49 48
D2 70 48 DIODE1
RPD2 49 70 5MEG
VIM9 70 72
RL 72 0 1000
CL 72 0 2.8PF
VIM8 42 40
R3 42 0 1000
LSER 42 0 1.8UH
VIM7 50 42
IRF 0 50 SIN(0 .4M 909MEG)
.MODEL DIODE1 D RS=10.0 IS=1.0E-14 N=1.0 CJO=.001PF VJ=.9 BV=20
.OPTIONS ACCT OPTS ITL3=10 LVLTIM=1 LIMPTS=20000 ITL5=40000
.TRAN 12.2070327.13PS .222US .111US
.PRINT TRAN V(70) I(VIM5) V(37,70) I(VIM8) V(40) V(0) V(0) V(0)
* Maximum parameters printed in one row is 8.
.END
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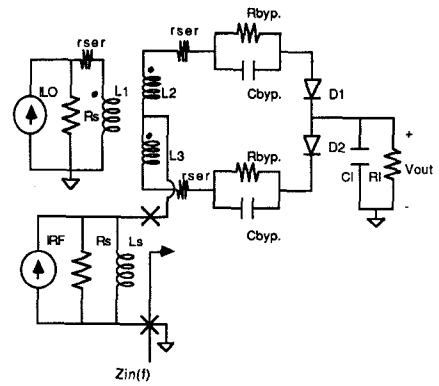

Figure 6. Resistively matched balanced mixer: circuit diagram and corresponding SPICE run file.

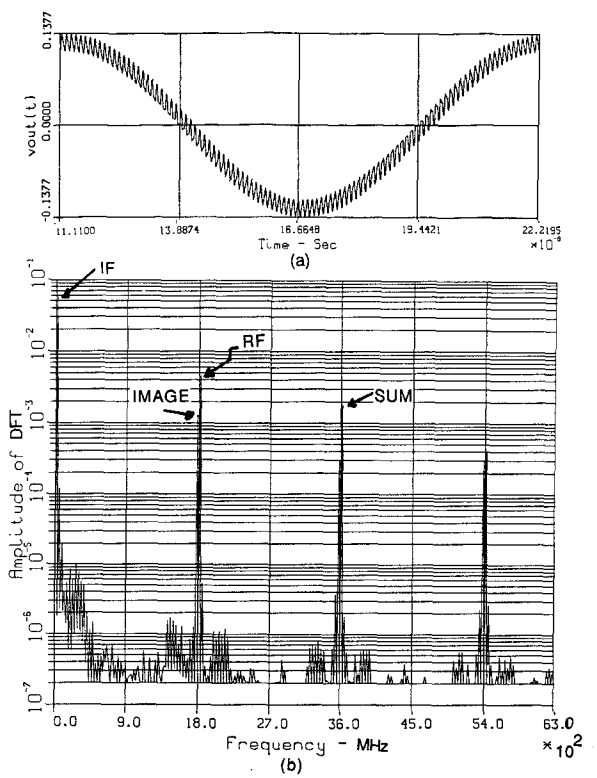

Figure 7. Output vout of the resistively matched balanced mixer: (a)time domain; (b)frequency domain.

MIXER DESIGN - DIODE WITH BARRIER RESISTANCE AND CAPACITANCE

Next the design of a low C_L mixer with a diode that possesses both nonlinear barrier resistance and capacitance is considered. Here time domain analysis provides a different perspective with which to examine the interaction of circuit and diode to optimize mixer performance. Although the frequency conversion process occurs predominately in the barrier resistance, R_B, parametric pumping of the barrier capacitance, C_B, is shown to enhance C_L. To maximize this effect a phasing circuit has been designed to time the energy flow between the diode's nonlinear capacitor, the matching circuit, and the diode's nonlinear resistor. This circuit will be described shortly. Applying these circuit techniques to our design problem, a broadband mixer circuit has been designed for devices with C_B's of .25pF and 1.0pF. C_L is 3.1dB and 4.25dB, respectively - close to the 3dB limit for resistive broadband mixers. In fact C_L under 3dB is now possible as both nonlinear elements are contributing to the conversion process. Noise performance is expected to be low as the conversion process is achieved in part by parametric pumping of the diode's capacitance. These results can be extended to mixers operating at higher frequencies provided that the diode parameters and reactive circuit elements are scaled according to frequency.

In Fig. 8, C_L is plotted as the diode's barrier capacitance at zero bias, C_{jo}, is varied from 0.0 to 1.0pF in three different circuits. These C_L performances are shown together to emphasize the benefits of optimizing performance using graphic criteria as well as linear circuit rules. The first curve plots C_L for the single-ended circuit of Fig. 3; uncompensated, the degradation in C_L with increasing C_B is high, demonstrating the need to design the circuit to a particular device. The second curve gives C_L obtained when inductive matching to C_B (L | | C_B) is performed. This is a very common compensation technique - it effectively treats C_B as though it had a fixed value. As a result, C_L decreases to a reasonable value although this C_L is 1.0 to 3.0dB worse than that of a resistive diode. The third curve shows C_L attained when the phasing circuit is used. The improvement over inductive matching is 1.5dB with C_{jo} = .25pF and 1.15dB with C_{jo} = 1.0pF.

The optimized single-ended mixer circuit for a device with C_{jo} = .25pF is shown in Fig. 9(a). The phasing circuit consists of a parallel inductor, L_1, and capacitor, C_2. L_1 is nominally chosen

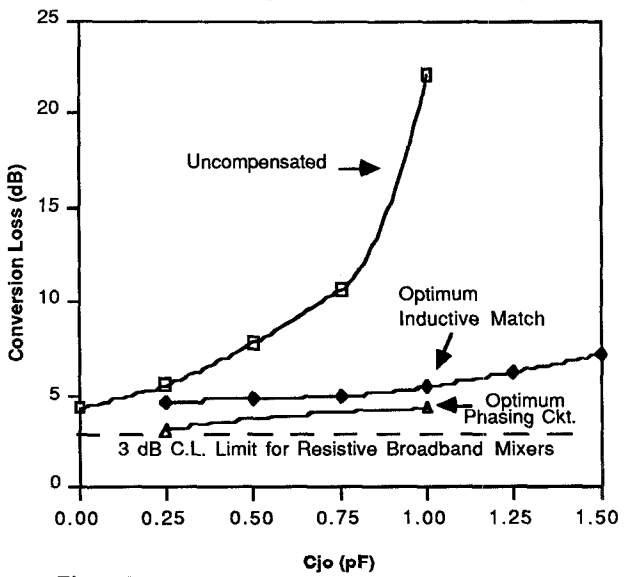

Figure 8. Conversion Loss vs. C_{jo}: (a)uncompensated; (b)optimum inductive matching; (c)optimum phasing circuit.

to resonate with $< C_B >$ at f_{RF}. If R_B were not present, the RF energy would alternate between L_1 and C_B. Turning the diode 'ON' upsets this pattern and allows I_{RF} to course through to the load. Our goal, as with the ideal switch, is to transfer as much current to the load when the diode is 'ON' and to keep T_{ON}/T_{LO} close to .50. To accomplish this, we store the RF energy when the diode is 'OFF' first in C_B then in L_1. Thus making this energy, in the form of I_{L1} available to the load when the diode turns 'ON'. The addition of C_2 helps control the point in the RF energy cycle when the diode turns 'ON'.

The top graph in Fig. 9(b) shows the energy pattern due to the LO, RF and bias sources. Energy transfer from C_B to L_1 to R_B in one LO cycle can be seen. This energy transfer is shown more clearly in the second graph as only the energy due to I_{RF} is plotted. The RF current components are plotted in the third graph; they are derived in the same way as those shown in Fig. 5. From this graph one observes that when the diode is turned 'ON' not all the RF source current flows in the diode. This effect can be reduced in the corresponding balanced mixer design; the C_L obtained for the case of C_{jo} = .25pF is 2.5dB.

Lastly we compare the results for the single-ended mixer design with and without barrier capacitance against those predicted using the conventional frequency domain analysis. Following the linear analysis based on Held and Kerr (5), we use our calculated values for the Fourier coefficient of the diode conductance and capacitance, G(f) and C_B(f), obtained from the FHT, and the embedding impedances provided by the circuit description as inputs in the small signal analysis. C_L is calculated to be 4.35dB and 3.5dB for the purely resistive case and that of C_{jo} = .25pF, respectively. Using Maas' computer program to solve the large signal and small signal problems, C_L is found to be 2.6dB and SSB noise temperature is 265 degrees in the C_{jo} = .25pF case(8).

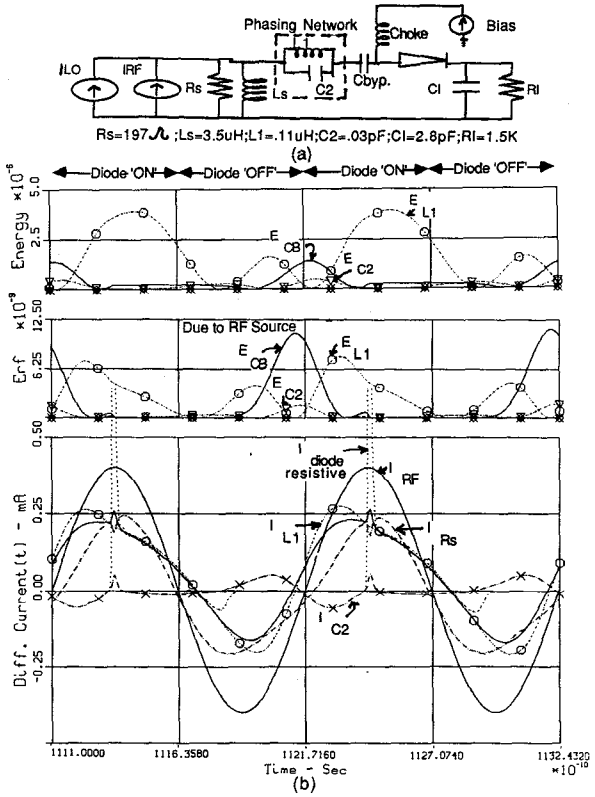

Figure 9. Optimized mixer when C_{jo}= .25pF;
(a)circuit diagram; (b)energy pattern and differential currents.

CONCLUSION

A computer-aided tool for mixer analysis and design, based on a time domain approach, has been presented. This technique uses SPICE to find the steady state solutions of the circuit waveforms and the Hartley transform to quickly evaluate circuit performance. The design tool described here differs from other time based analysis in that it is not confined to a particular circuit (1) or to a specific ratio of input/output frequencies (7). It is the first report, to the authors' knowledge, of a general purpose time domain design tool. In addition, the direction for circuit optimization is specified by considering not only linear circuit guidelines but also graphic criteria. Using this tool, circuits were designed for mixers with diodes possessing nonlinear barrier resistance and capacitance. They show frequency conversion due to both nonlinear elements. Similar results have been reported in the literature (3), although this contradicts the commonly held belief that addition of barrier capacitance in the diode model degrades mixer conversion loss and noise figure (9,4). It is hoped that this tool can be used to design circuits which take advantage of the nonlinearities of C_B and R_B to improve C_L and that the results presented here will motivate new discussion on the optimization of downconverter performance with C_B.

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